Description

The HX215028 is a 25-watt, highly rugged, unmatched LDMOS FET, designed for wide-band commercial and industrial applications at frequencies HF to 1.5 GHz. It can be used in Class AB/B and Class C for all typical modulation formats.

HX215028

• Typical Performance (On fixture with device soldered):
V_{DD} = 28 Volts, I_{DQ} = 150 mA, CW.

Frequency	Gp (dB)	P_{-1dB} (W)	$\eta_D@P_{-1}$ (%)
1000 MHz	20	25	60

• Typical Performance (In Demo Fixture): V_{DD} = 24 Volts, I_{DQ} = 50 mA, CW.

Frequency	Gp (dB)	P_{OUT} (W)	η_D (%)	2nd Harmonic (dBc)	3rd Harmonic (dBc)
1300 MHz	14.5	21	50	-18	-29

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)
- 470-860MHz (TV UHF)
- 100kHz - 1000MHz (ISM, instrumentation)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+95	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+50	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	1.5	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class

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Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

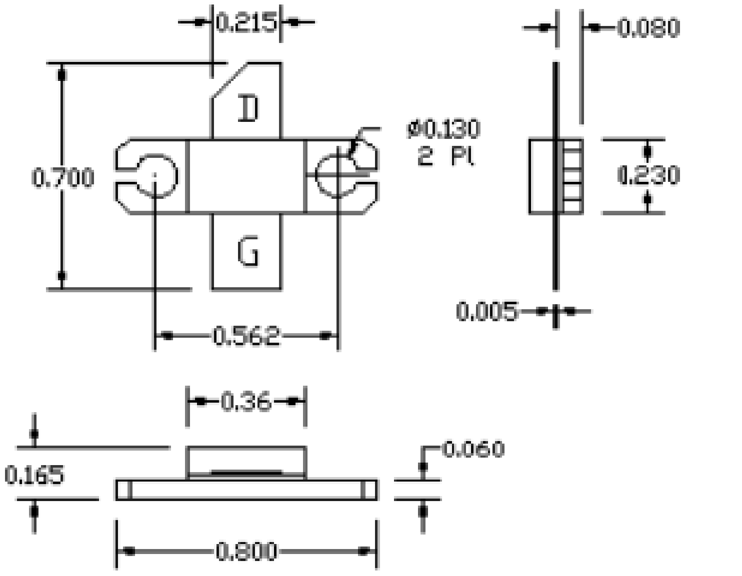
Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$	95	97		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 75V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 150 μA)	V_{GS}(th)	——	2.11	——	V
Gate Quiescent Voltage (V_{DD} = 28 V, I_D = 150 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.0	——	V
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{ISS}		31.5		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{OSS}		12.8		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =28 V, f = 1 MHz)	C_{RSS}		0.7		pF
Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 150mA, f = 1000 MHz, CW Signal Measurements.					
Power Gain	Gp	——	20	——	dB
Drain Efficiency@P1dB	η_D	——	60	——	%
1 dB Compression Point	P_{-1dB}	——	25	——	W
Input Return Loss	IRL	——	-7	——	dB

Load Mismatch (In Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 150 mA, f = 1000 MHz

VSWR 20:1 at 25W pulse CW Output Power	No Device Degradation

Package Outline

Flanged ceramic package; 2 leads



Tolerance .XX +/-0.01 .XXX +/-.005 inches

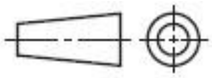
OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-G2E					03/12/2013

Figure 1. Package Outline PKG-G2E