HX505300VX

Description

The HX505300VX is a 250-watt capable, high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 0.5 GHz.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as FM radio, VHF TV and Aerospace applications.

- Typical performance (on test board with device soldered)

  Signal: CW, Vgs=3.38V, Vds=50V, Idq=120mA

Freq(MHz)	Pin(dBm)	Pout(W)	IDS(A)	Gain(dB)	Eff(%)
110	36.2	214	6.18	17.1	69
120	36.2	234	6.68	17.5	70
130	35.9	218	6.29	17.48	69
140	36	228	6.52	17.58	70
150	35.9	238	6.47	17.86	73
160	35.8	229	5.85	17.8	78

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 160-230MHz (TV VHF III)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+125	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.60	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

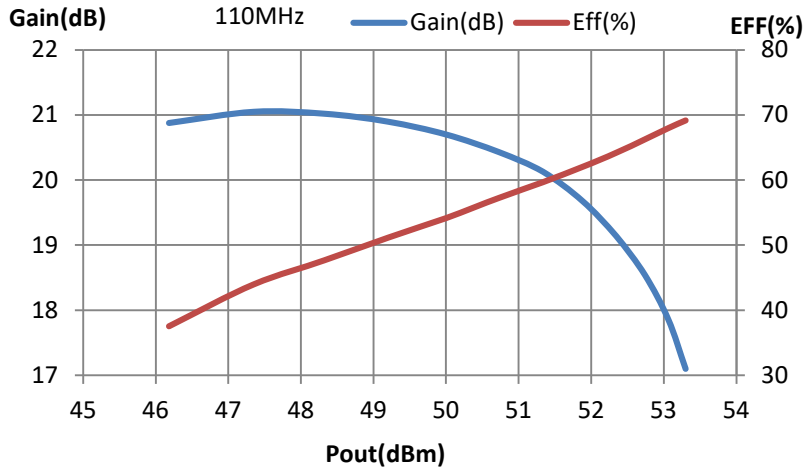
Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (per half section)					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$		125		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 75V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	——	2.65	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 100 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.1	——	V
Drain source on state resistance (Vds=0.1V, Vgs=10V)	Rds(on)		217		mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{ISS}		158		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{OSS}		46.8		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{RSS}		1.24		pF

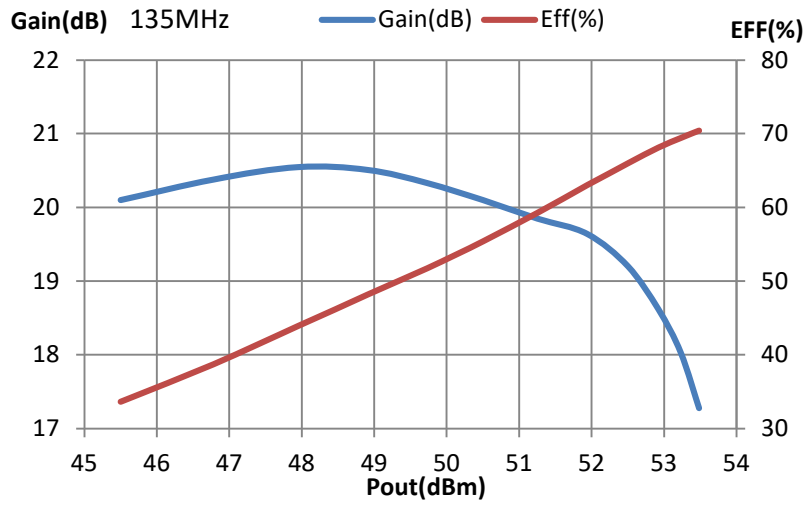
Load Mismatch (In Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 100 mA, f =160MHz, pulse width:100us, duty cycle:10%

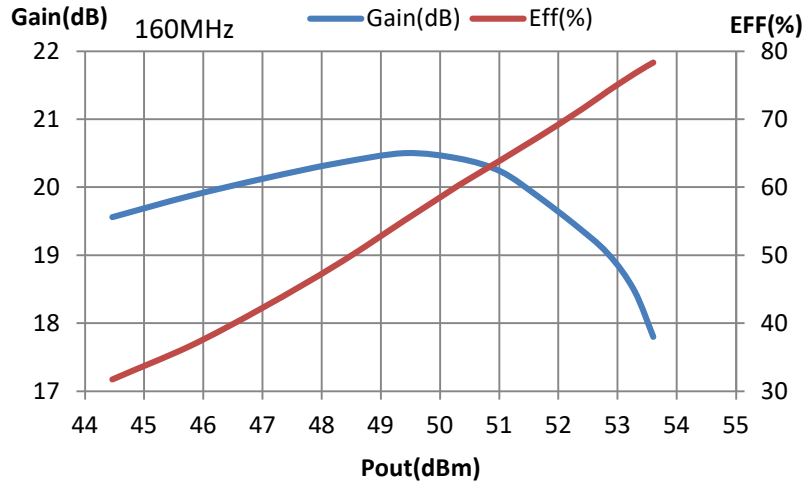
Load 20:1 All phase angles, at 250W Pulsed CW Output Power	No Device Degradation

TYPICAL CHARACTERISTICS

Figure 1: CW Gain and Power Efficiency as a Function of Pout across 110-160MHz







Reference Circuit of Test Fixture Assembly Diagram
(30mil TC350)

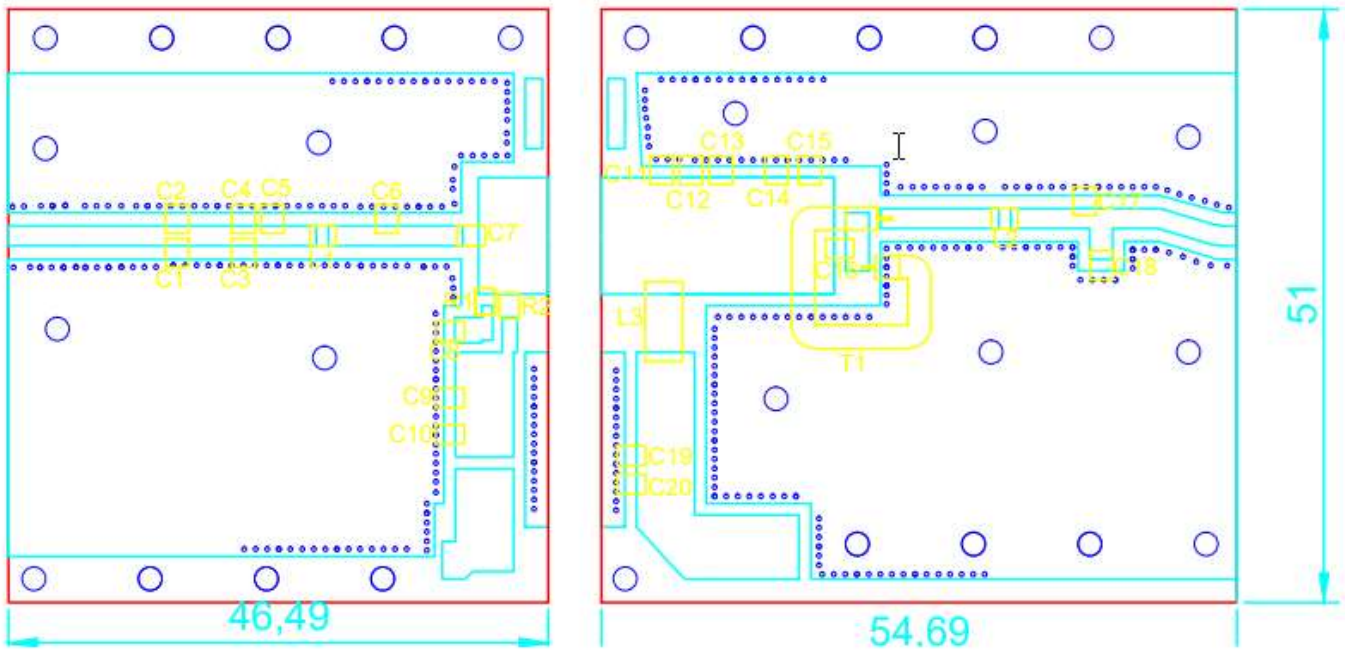
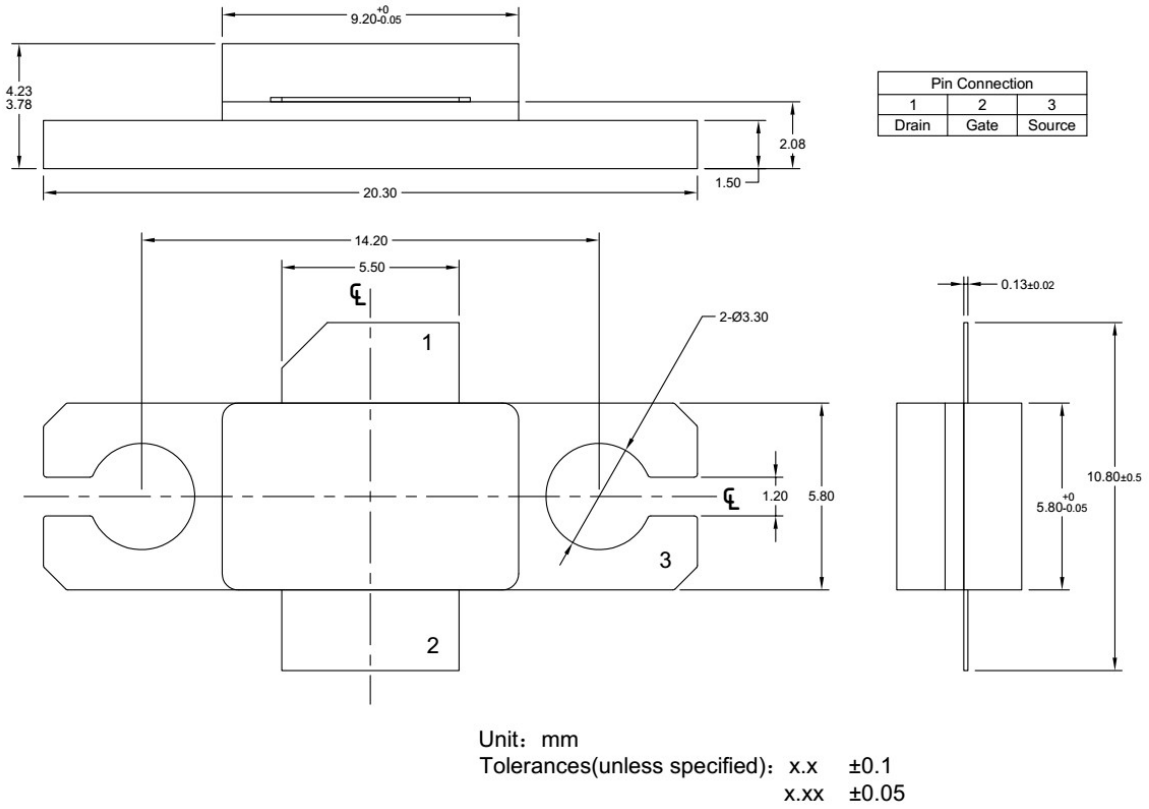


Table 5. Test Circuit Component Designations and Values

Part	Description	Model
C1,C2,C3,C4,C17,C18	9.1pF	ATC800B
C5,C14	5.1pF	ATC800B
C6	39pF	ATC800B
C7,C8,C19	10nF	C4532X7R3D103KT000N
C9,C16	1000pF	ATC800B
C11,C12,C13,C15	10pF	ATC800B
C10,C20	10uF	10Uf/50V
R1	75Ω	0805
R2	39Ω	0805
L1	22nH	0805
L2	1 turn, line length= 10mm	
L3	16 turns, diameter=5mm	
T1	50Ω, line length=115mm	SF-086-50

Package Outline

Flanged ceramic package; 2 leads



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-GXB					10/10/2017

Figure 1. Package Outline PKG-G2E